89C024LT
ERROR CORRECTING LAPTOP MODEM CHIP SET

- CHMOS for Low Operating Power
- Low Standby Power Requirements
- Minimum Chip Count for Small size
- MNP* Operation through Class 4 for Error Correction
- MNP Class 5 Data Compression for Increased Throughput
- AT Command Set
- V.22 bis, V.22 A/B, V.21, Bell 212A, and Bell 103 Compatible
- For Public Switched Telephone Network and Unconditioned Leased Line Applications
- Automatically Detects Remote Modem Type and Data Rate
- On-Chip Hybrid
- DTMF and Pulse Dialing
- On-Chip Serial Port and Handshake Signals for RS-232/V.24 Interface
- Serial Interface to External NVRAM
- Automatic Speed Matching in MNP and Normal Modes
- Hardware and Software Flow Control
- Analog/Digital Loopback Diagnostics
- Telephone Line Audio Monitor Output
- Full Set of Control Signals for DAA Interface
- International Call Progress Tone Detection Capabilities
- Automatic Adaptive Equalization
- Synchronous Modes
- Easily Customized Command Set and Features
- Intel's MNP Software Co-Developed with R. Scott Associates**
- Packaging:
  - — For Packages
    QN89026LT SV782 68-Pin PLCC
    QN89027 28-Pin PDIP
    Order Kit #89C024LT SZ504
  - — For Packages
    QN89026LT SV782 68-Pin PLCC
    QN89027 28-Pin PLCC
    Order Kit #89C024LT SZ505

(See Packaging Specifications Order Number 240800-001)

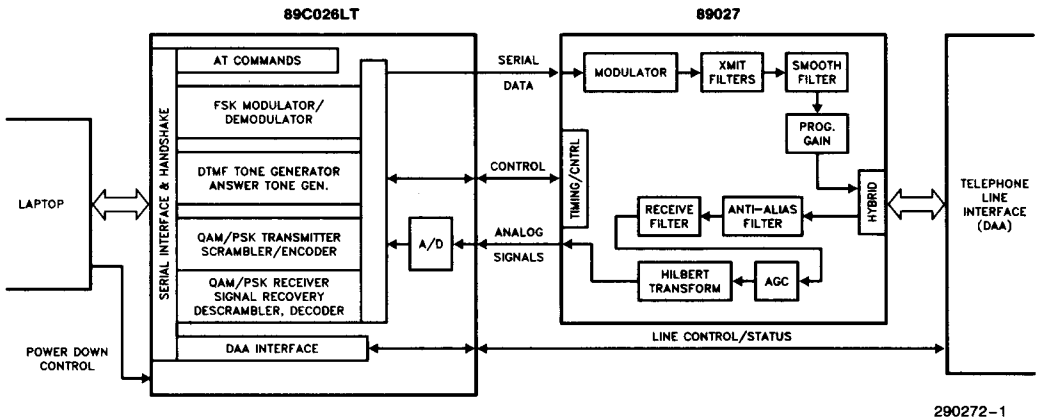

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Figure 1. 89C024LT System Block Diagram

*MNP is a registered trademark of Microcom, Inc.
**R. Scott Associates, Inc., 5711 Six Forks Road, Suite 301, Raleigh, North Carolina 27609, (919) 846-7171

October 1993
Order Number: 290272-005

GENERAL DESCRIPTION

Intel 89C024LT is a highly integrated, low power, error correcting laptop modem chip set. This two chip solution is composed of the 89027 Analog Front End and 89C026LT microcontroller. At 12.96 MHz the microcontroller is capable of executing error correction and data compression routines. The system is compatible with the following CCITT and BELL standards.

- CCITT V.22 bis
  2400 bps sync and async
  1200 bps sync and async
- CCITT V.22 A & B
  1200 bps sync and async
- CCITT V.21
  0 to 300 bps anisochronous
- BELL 212A
  1200 bps sync and async
  300 bps fall-back mode
- BELL 103
  0 to 300 bps anisochronous

The 89C024LT system consists of a 16 bit application specific processor (89C026LT) and an analog front end device (89027). The 89C026LT processor performs all "Digital Signal Processing" algorithm execution for processing the modem signals, as well as providing all modem control functions typically performed by an external processor. The analog front end provides for 2 wire and 4 wire telephone line interface, D/A conversion, and most of the complex filtering functions required in QAM/PSK/FSK modems. Refer to Figure 1 for a simplified block diagram of the system.

In laptop modem applications, the 89C024LT chip set along with a Data Access Arrangement (DAA), a single 8-bit EPROM, and an 8K x 8 static RAM represent the circuitry required for implementing an auto-dial, auto-answer, 300 to 2400 bps, MNP class 5 full duplex intelligent modem. Refer to Figure 2 for a block diagram of this application.

A complete set of Industry Standard AT commands is provided for modem configuration and user interface. Additional commands have been implemented for power down modes and MNP feature control. Virtually all PC software written for the AT command set can also be used with this chip set. Alternatively, in applications where user proprietary modem control commands and features are desired, the user can replace the 89C024LT command module with custom proprietary software.

The 89C024LT has a set of default features. Upon power up, the modem configuration will be in accordance with these default options, unless a different configuration has been saved in optional external NVRAM with the &W command.

The 89C024LT modem has built in auto-dialing and auto-answering capabilities. It can be configured to the proper line signaling mode (Tone or Pulse), and to the type (CCITT or Bell) and speed of the calling or answering modem. It can also detect and identify call set-up signals of telephone networks, allowing unattended data call operation.

A full set of diagnostic loop-test features compatible with CCITT V.54 is supported. The chip set also provides a line signal for audio monitoring of call progress, a comprehensive set of DAA control lines for a simple interface to the telephone network, and a full complement of TTL level RS-232/V.24 handshake signals.

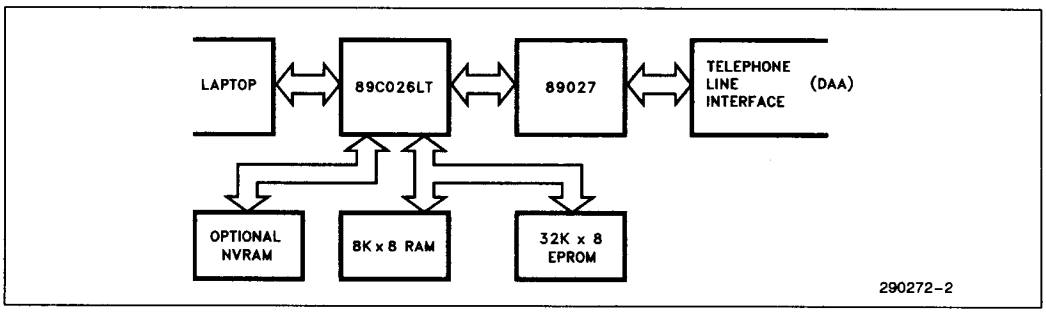

Figure 2. 89C024LT Laptop Modem Application

PACKAGING

89027 is available in PLCC and standard plastic DIP packages. The 89C026LT is available in a PLCC package. Packages are shown from top view, looking down on component side of PC board.

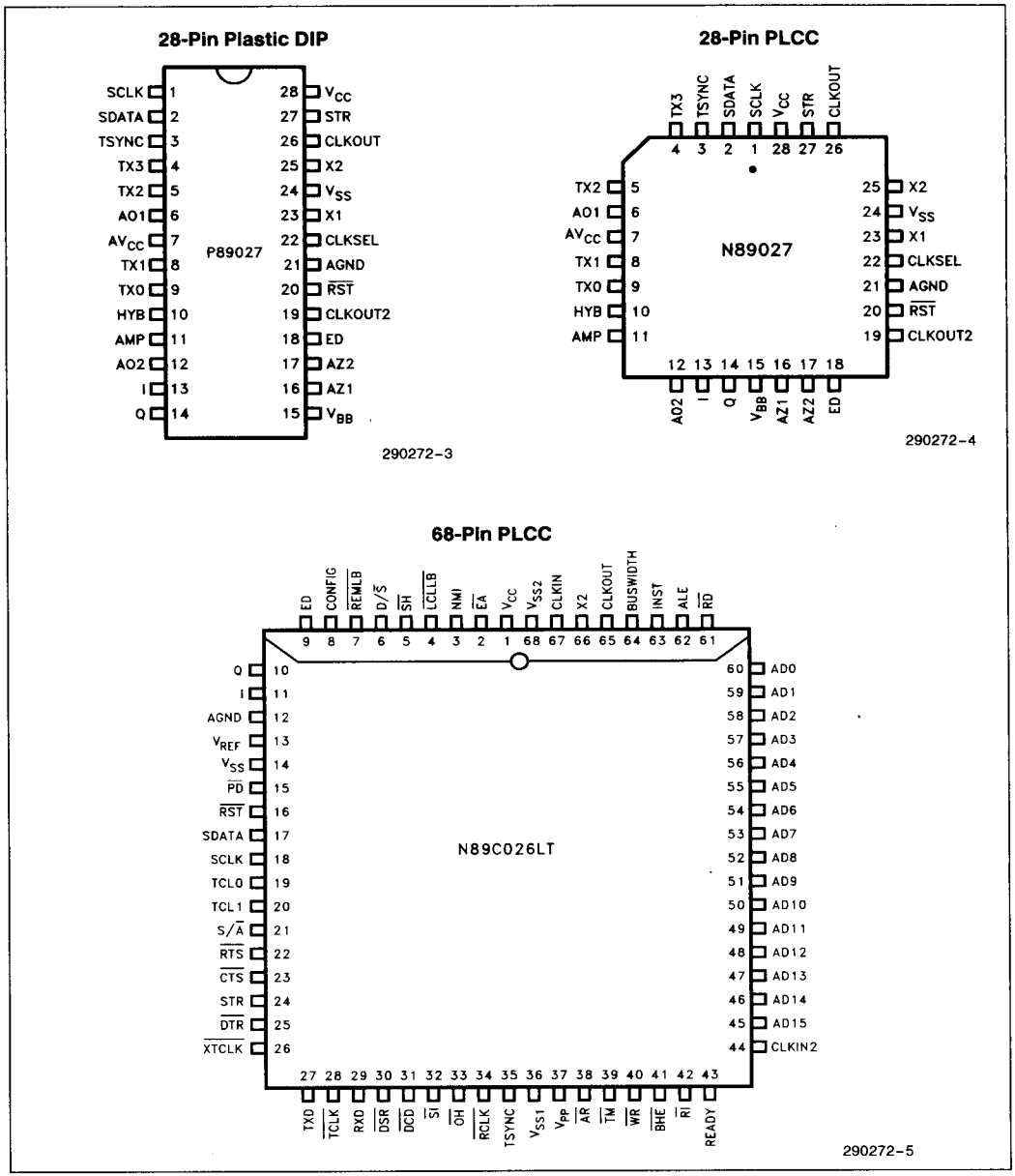

Figure 3. Device Packages

CALL ESTABLISHMENT, TERMINATION AND RETRAIN

The 89C024LT modem system incorporates all protocols and functions required for automatic or manual call establishment. The modem system also incorporates all protocols and functions required for progress and termination of a data call.

The modem chip set has a built-in auto-dialer, both DTMF and Pulse type. It can detect dial, busy, and ringback signals from the remote end, and will provide call progress messages to the user. The modem is also capable of re-dialing the last number dialed.

The modem, when configured for auto-answer, will answer an incoming call, remain silent for the two second billing delay interval, and then transmit the answer tones. Afterwards modem to modem identification and handshaking will proceed at a speed and operating mode acceptable to both ends of the link.

The data call can also be setup by manual dialing. A transition from voice (i.e., for the purpose of manual dialing) to data mode can be done by the use of a mechanical switch (exclusion key) on the $\overline{SH}$ pin. Once set to data mode, the modem handshaking will proceed before the modems will be ready to accept and exchange data.

During data transmission, if one of the modems finds that the received data is likely to have a high bit error rate (indicated by a large mean square error in the adaptive equalizer), it initiates a retrain sequence. This automatic retrain feature is only available at 2400 bps, and is compatible with CCITT V.22 bis recommendations.

Disconnection of the data call can be initiated by the DTE at the local end or by the remote DTE (if the modem is configured to accept it). Whether $\overline{DTR}$ will initiate a disconnect depends on the last &D command. Receiving a long space from a remote modem will initiate a disconnect only after a Y1 command. The optional disconnect requests, originated by the remote modem, are of two types, (1) disconnect when receiving long-space, and (2) disconnect when received carrier is dropped. The modem chip set can also be configured to transmit "long-space" just before disconnection.

Because the CCITT and Bell modem connection protocols do not provide recognition of remote modem type (i.e. V.22 bis to 212A), the Intel chip set provides the additional capability of identifying the remote modem type. This feature is beneficial during the migration phase of the technology from the 1200 bps to 2400 bps. In North America, where the installed base of 1200 bps modems is mostly made-up of 212A type, this feature allows a "Data Base Service Provider" to easily upgrade the existing 212A modems to 2400 bps V.22 bis standard, transparently, to 212A users. Similarly, a user with a 89C024LT based modem system can automatically call data bases with either 212A or V.22 bis modems, without concern over the difference. This feature's benefits are realized in smooth upgrading of data links, with minimum cost and reduced disruption in services. Refer to Table 1 for a detailed description of remote modem compatibility.

SOFTWARE CONFIGURATION COMMANDS

This section lists the 89C024LT commands and registers that may be used while configuring the modem. Commands instruct the modem to perform an action, the value in the associated registers determine how the commands are performed, and the result codes returned by the modem tell the user about the execution of the commands.

The commands may be entered separately or in string fashion. Any spaces within or between commands will be ignored by the modem. During the entry of any command, the 'backspace' key (CNTRL H) can be used to correct any error. Upper case or lower case characters can be used in the commands. Commands described in the following paragraphs refer to asynchronous terminals using ASCII codes.

Table 1. Remote Modem Compatibility

Originating 89C024LT Modem		Answering Modem: Bell 300	Bell 1200	CCITT 300	CCITT 1200	CCITT 2400
Bell	300	300	300	—	300*	300*
	1200	1200*	1200	—	1200	1200
CCITT	300	—	—	300	—	—
	1200	1200*	1200	—	1200	1200
	2400	1200*	1200		1200	2400

Answering 89C024LT Modem		Originating Modem: Bell 300	Bell 1200	CCITT 300	CCITT 1200	CCITT 2400
Bell	300	300	1200	—	1200	1200
	1200	300	1200	—	1200	1200
CCITT	300	—	—	300	—	—
	1200	300*	1200	—	1200	1200
	2400	300*	1200	—	1200	2400

* These connection data rates are obtained when connecting 89C024LT based modems end to end. The same results may not be obtained when a 89C024LT based modem is connected to other modems.

1

Command Set

AT	Attention code.
A	Go off-hook in answer mode
A/	Repeat previous command string
Bn	BELL/CCITT Protocol Compatibility at 300 and 1200 bps
Ds	The dialing commands (0-9 A B C D * # P R T S W , ; @)
En	Echo command (En)
Hn	Switch-Hook Control If &J1 option is selected, H1 will also switch the auxiliary relay
In	Request Product Code and Checksum
Ln	Speaker Volume
Mn	Monitor On/Off
O	On-Line
Qn	Result Codes
Sn=x	Write S Register
Sn?	Read S Register
Vn	Enable Short-Form Result Codes
Xn	Enable Extended Result Code
Yn	Enable Long Space Disconnect
Z	Fetch Configuration Profile
+++	The Default Escape Code

MNP Feature Control Command Set

\An	Maximum MNP Block Size
%An	Set Auto-Reliable Fallback Character
\Bn	Transmit Break
\Cn	Set Auto-Reliable Buffer
%Cn	Set MNP Compression
\Gn	Set Modem Port Flow Control
\Jn	Bits per Second Rate Adjust
\Kn	Set Break Control
\Nn	Set Operating Mode
\O	Originate Reliable Link
\Qn	Set Serial Port Flow Control
\S	View Active Configuration
\Tn	Set Inactivity Timer
\U	Accept Reliable Link
\Vn	Modify Result Code Form
\Xn	Set XON/XOFF Pass-Through
\Y	Switch to Reliable Mode
\Z	Switch to Normal Mode

& Command Set

&Cn	DCD Options
&Dn	DTR Options
&Fn	Fetch Factory Configuration Profile
&Gn	Guard Tone
&Jn	Telephone Jack Selection
&Ln	Leased/Dial-up Line Selection
&Mn	Async/Sync Mode Selection
&Pn	Make/Break Pulse Ratio
&Rn	RTS/CTS Options
&Sn	DSR Options
&Tn	Test Commands
&Wn	Write Configuration to Non Volatile Memory
&Xn	Sync Clock Source
&Yn	Default NVRAM Profile Select
&Zn	Store Telephone Number

+ Command Set

+En	Disable/Enable Power Down
+Tn	Time to Power Down

CONFIGURATION REGISTERS

The modem stores all the configuration information in a set of registers. Some registers are dedicated to a special command and function, and others are bit-mapped, with different commands sharing the register space to store the command status.

S0*	Ring to Answer
S1	Ring Count. (Read Only)
S2	Escape Code Character
S3	Carriage Return Character
S4	Line Feed Character
S5	Back Space Character
S6	Wait for Dial Tone
S7	Wait for Data Carrier
S8	Pause Time for the Comma Dial Modifier
S9	Carrier Detect Response Time
S10	Lost Carrier to Hang Up Delay
S11 *	DTMF Tone Duration
S12	Escape Code Guard Time
S13	Not Used
S14 *	Bit Mapped Option Register
S15	Not Used
S16	Modem Test Options
S17	Not Used
S18 *	Test Timer
S19	Not Used
S20	Not Used
S21 *	Bit Mapped Options Register
S22 *	Bit Mapped Options Register
S23 *	Bit Mapped Options Register
S24	Not Used
S25 *	Delay to DTR (Sync Only)
S26 *	RTS to CTS Delay (Half Dup.)
S27 *	Bit Mapped Options Register
S31 *	Bit Mapped Options Register

NOTE:
* These S registers can be stored in the NVRAM.

DIALING

Dial modifiers are available for adding conditions to dialed phone numbers.

Dial Modifiers

P	Pulse Dial
R	Originate call in Answer Mode
T	Tone Dial
S	Dial a stored number
W	Wait for dial tone
,	Delay a dial sequence
;	Return to command state
!	Initiate a flash
@	Wait for quiet

Example:

Terminal: AT &Z0 = T 1 (602) 555-1212
Modem: OK

Result: Modem stores the Tone Dial (T) modifier and phone number T16025551212 in the external NVRAM.

The number can be dialed from asynchronous mode by issuing the following command:

Terminal: AT DS0
Modem: T16025551212

Result: Modem dials phone number and attempts to establish a connection.

or by turning on $\overline{DTR}$ when in Synchronous Mode 2. Up to 33 symbols (dial digits and dial modifiers) may be stored. Spaces and other delimiters are ignored and do not need to be included in the count. If more than 33 symbols are supplied, the dial string will be truncated to 33.

POWER MANAGEMENT

The flexible power management controls allow for a variety of command and hardware driver options. The power down sequence is initiated by placing a logic "low" on pin 15 ($\overline{PD}$) of the 89C026LT. The laptop can control the $\overline{PD}$ signal directly. If such a signal is unavailable, $\overline{PD}$ can be controlled by communications software via $\overline{DTR}$. Lack of data activity or an in-coming ring signal can also be used to control $\overline{PD}$.

Placing the crystal on the 89C026LT (Figure 10) allows it to reduce power consumption by turning off the oscillator. When online and connected to a remote modem, the power consumption for the 89C024LT is typically 400 mW. Additionally, when the 89027 is not needed (on-hook, not connected to a remote modem) the 89C026LT places it in standby. In standby the chip set power consumption is typically 255 mW. When powered down via the $\overline{PD}$ pin on the 89C026LT, the chip set typically consumes 5 mW. Minimum memory-system power-consumption can be achieved by chip selecting memory only when addressed.

APPLICATIONS OVERVIEW

The block diagram of a stand-alone 300 to 2400 bps Hayes compatible modem is depicted in Figure 4. The DAA section shown in this diagram may be implemented using the suggested diagram in Figure 5. Figure 6 shows the use of the power-down feature.

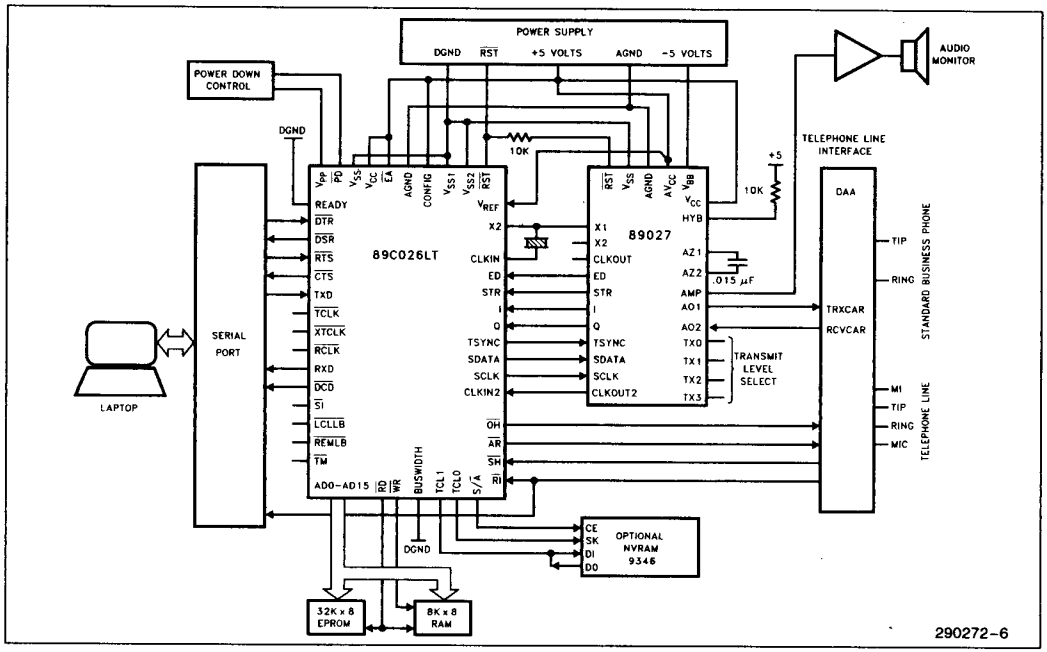

Figure 4. Typical Laptop Modem

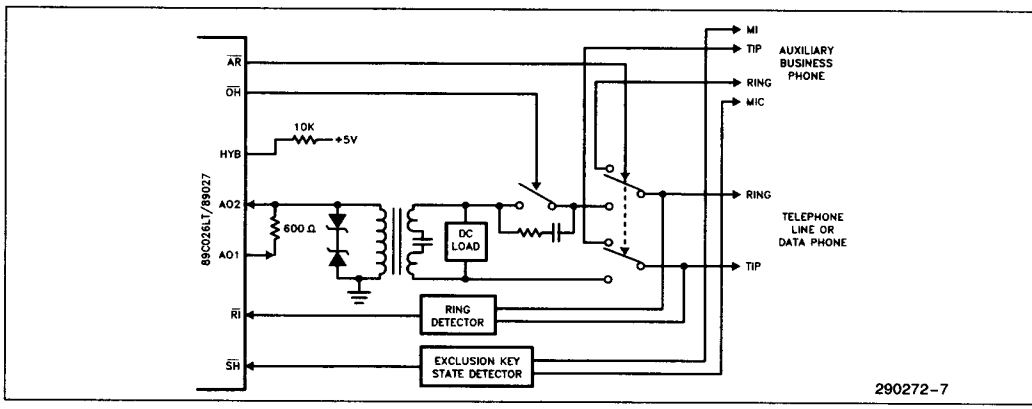

Figure 5. Typical Telephone Line Interface Using Internal Hybrid

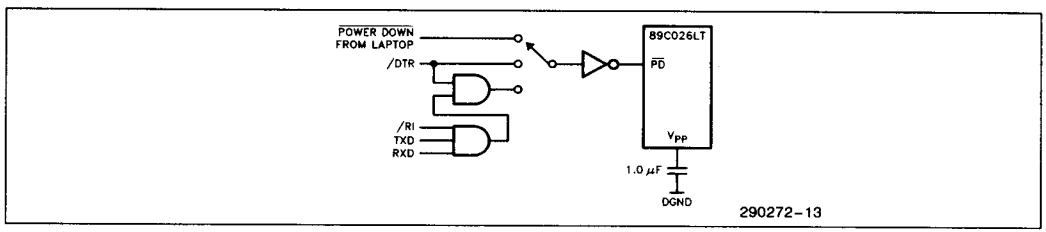

Figure 6. Power-Down Control

SYSTEM COMPATIBILITY SPECIFICATIONS

Parameter	Specification
Synchronous	2400 bps ±0.01% V.22 bis 1200 bps ±0.01% V.22 and BELL 212A
Asynchronous	2400, 1200 bps, character asynchronous. 0 - 300 bps anisochronous.
Asynchronous Speed Range	+1% −2.5% default. Extended +2.3% −2.5% range of CCITT standards optional via software customization.
Asynchronous Format	10 bits, including start, stop, parity. (8, 9, 11 bits optional via S/W customization.)
Synchronous Timing Source	a) Internal, derived from the local oscillator. b) External, provided by DTE through XTCLK. c) Slave, derived from the received clock.
Telephone Line Interface	Two wire full duplex over public switched network or 4 wire leased lines. On-chip hybrid and billing delay timers.
Modulation	V.22 bis, 16 point QAM at 600 baud. V.22 and 212A, 4 point PSK at 600 baud. V.21 and 103, binary phase coherent FSK
Output Spectral Shaping	Square root of 75% raised cosine, QAM/PSK.
Transmit Carrier Frequencies V.22 bis, V.22, 212A V.21 Bell 103 mode	 Originate 1200 Hz ± .02% Answer 2400 Hz ± .02% Originate 'space' 1180 Hz ± .02% Originate 'mark' 980 Hz ± .02% Answer 'space' 1850 Hz ± .02% Answer 'mark' 1650 Hz ± .02% Originate 'space' 1070 Hz ± .02% Originate 'mark' 1270 Hz ± .02% Answer 'space' 2020 Hz ± .02% Answer 'mark' 2225 Hz ± .02%
Received Signal Frequency Tolerance V.22 bis, V.22, 212A V.21 Bell 103	 Originate 2400 Hz ± 7 Hz Answer 1200 Hz ± 7 Hz Originate 'space' 1850 Hz ± 12 Hz Originate 'mark' 1650 Hz ± 12 Hz Answer 'space' 1180 Hz ± 12 Hz Answer 'mark' 980 Hz ± 12 Hz Originate 'space' 2020 Hz ± 12 Hz Originate 'mark' 2225 Hz ± 12 Hz Answer 'space' 1070 Hz ± 12 Hz Answer 'mark' 1270 Hz ± 12 Hz
Typical Energy Detect Sensitivity	Greater than −43 dBm ED is ON. Less than −48 dBm ED is OFF. Signal in dBm measured at AO2.
Energy Detect Hysteresis	A minimum Hysteresis of 2 dB for QAM scrambled mark.
Line Equalization	Fixed compromise equalization, transmit. Adaptive equalizer for PSK/QAM, receive.
Diagnostics Available	Local analog loopback. Local digital loopback. Remote digital loopback.
Self Test Pattern Generator	Alternate 'ones' and 'zeros' and error detector, to be used along with most loopbacks. A number indicating the bit errors detected is sent to DTE.

RECEIVER PERFORMANCE SPECIFICATIONS

Test Cases		Typical SNR for 10^{-5} BER Performance	
Data Mode	Rx Level (dBm)	Answer (dB)	Originate (dB)
V.22 bis Synchronous	−30	16	16.5
	−40	16.5	18
V.22/Bell 212A Synchronous	−30	6.5	6.5
	−40	6.5	6.5
V.21 Asynchronous	−30	9	7.5
	−40	9	8
Bell 103 Asynchronous	−30	10	11.5
	−40	10	11.5

Test Conditions:

— Receive Signal (Rx) measured at A02 (transmit level set at −9 dBm)

— Unconditioned 3002 Line

— 3 KHz Flat-Band Noise

PERFORMANCE SPECIFICATIONS

Parameter	Min	Typ	Max	Units	Comments
DTMF Level		4.0		dBm	at AO1
DTMF Second Harmonic			−35	dB	HYB enabled into 600Ω
DTMF Twist (Balance)		3		dB	
Default DTMF Duration		100		ms	Software Controlled
Pulse Dialing Rate		10/20		pps	Software Controlled
Pulse Dialing Make/Break		39/61 33/67		% %	US UK, Hong Kong
Pulse Interdigit Interval		785		ms	
Billing Delay Interval			2.1	sec	
Guard Tone Frequency Amplitude Frequency Amplitude		540 −3 1800 −6		Hz dB Hz dB	referenced to High Channel transmit. QAM/PSK Modes Only
Dial Tone Detect Duration		3.0		sec	
Ringback Tone Detect Duration Cadence		 0.75 1.5		 sec 	 Off/On Ratio
Busy Tone Detect Duration Cadence	 0.67	 0.2 	 1.5	 sec 	 Off/On Ratio

89C026LT OVERVIEW

The 89C026LT processor performs data manipulation, signal processing and user interface functions. It requires a single ROM and RAM to execute standard, and/or custom code with high level protocol functions. A block diagram of the 89C026LT is provided in Figure 7.

89C026LT contains a TTL compatible serial link to DTE equipment, along with a full complement of V.24/RS-232-C control signals. A UART or USART may be used to transfer data to and from a microcomputer bus. The 89C026LT supports the industry standard AT command set facilitating compatability with most PC software.

During transmit operation, the 89C026LT synthesizes DTMF tones and the 300 BPS FSK modem signal and transmits them to the 89027 as digitized amplitude samples. During 1200 and 2400 BPS operation, DPSK and QAM is used to send 2 to 4 bits of information respectively at 600 baud to the AFE. Because the QAM coding technique is an inherently synchronous transmission mechanism, in the case of asynchronous QAM transmission, the asynchronous data is synchronized by adding or deleting stop bits. Following the synchronization process, the 89C026LT transmits digitized phase and amplitude samples to 89027 over the high speed serial link.

In the receive operation, the information is received by the 89C026LT from the 89027 as two signals which are 90 degrees phase shifted from each other. These analog signals are then digitized by the A/D converter resident on the 89C026LT. By using DSP algorithms, the received signals are processed using adaptive equalization for telephone line delay, amplitude distortion and gain adjustments and the signal demodulated. Following demodulation, the data is unscrambled, and if necessary, returned to asynchronous format.

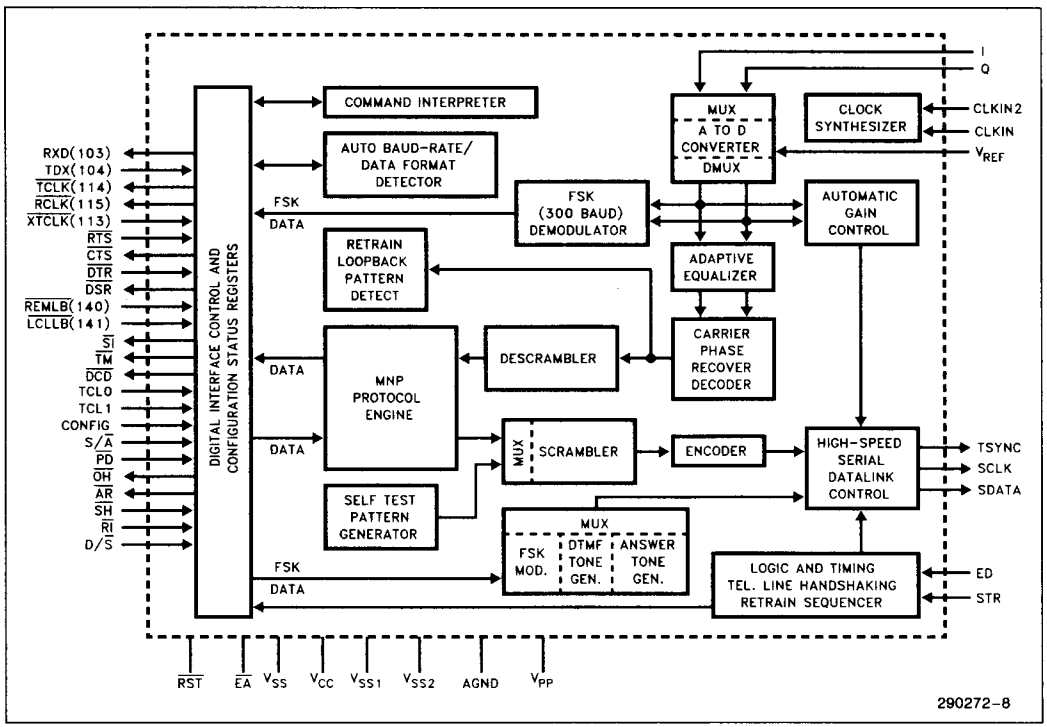

Figure 7. 89C026LT Block Diagram

89C026LT PINOUT

Symbol	Function (89C024LT)	Direction(4)	Pin No.
CLKIN	12.96 MHz master clock from 89027	In	67
CLKIN2	270 KHz from 89027	In	44
$\overline{RST}$	Chip reset (active low)	In	16
I	In-phase received signal	In	11
Q	Quadrature-phase received signal	In	10
STR	Symbol Timing from 89027	In	24
ED	Energy Detect input	In	9
TSYNC	Transmitter sync pulse to 89027	Out	35
SDATA	Serial Data to 89027	Out	17
SCLK	Serial Clock to 89027	Out	18
$\overline{OH}$	Off-Hook control to DAA	Out	33
$\overline{SH}$	Switch-Hook from dataphone	In	5
$\overline{RI}$	Ring Indicator from DAA	In	42
$\overline{AR}$	Aux Relay control to DAA	Out	38
TCL1	NVRAM Data I/O	I/O	20
TCL0	NVRAM CLK	Out	19
$\overline{PD}$	Power-down control	In	15
S/$\overline{A}$	NVRAM $\overline{CE}$	Out	21
D/$\overline{S}$	Dumb/$\overline{Smart}$ mode select	In	6
CONFIG	Reserved for future use (V_{CC})(2)	In	8
$\overline{TM}$	Test Mode Indicator	Out	39
TXD	Transmitted data from DTE	In	27
RXD	Received data to DTE	Out	29
$\overline{RTS}$	Request to send from DTE	In	22
$\overline{CTS}$	Clear to Send to DTE	Out	23
$\overline{DSR}$	Data Set Ready to DTE	Out	30
$\overline{DCD}$	Data Carrier Detect to DTE	Out	31
$\overline{DTR}$	Data Terminal Ready from DTE	In	25
$\overline{RCLK}$	Received clock to DTE	Out	34
$\overline{TCLK}$	Transmit clock to DTE	Out	28
$\overline{XTCLK}$	External timing clock from DTE	In	26
$\overline{SI}$	Speed Indicator to DTE	Out	32
$\overline{REMLB}$	Remote Loopback Command from DTE	In	7
$\overline{LCLLB}$	Local Loopback Command from DTE	In	4
V_{CC}	Positive power supply (+5V)	+5V	1
V_{SS}	Digital Ground	GND	14
V_{REF}	A/D converter reference	+5V	13
V_{SS1}	Digital ground	GND	36
V_{SS2}	Digital ground	GND	68
AGND	Analog ground	AGND	12
V_{PP}	Timing pin for return from power-down	In	37
$\overline{EA}$	External Memory enable	In	2
AD0-AD15	External memory access address/data(3)	I/O	60–45
$\overline{AA}$	Auto Answer(3)	Out	60
$\overline{JS}$	Jack Select(3)	Out	59
$\overline{CD}$	Carrier Detect Indicator(3)	Out	58
$\overline{MR}$	Modem Ready Indicator(3)	Out	57
$\overline{REL}$	MNP Reliable Link Active(3)	Out	56
$\overline{CLASS5}$	MNP Class 5 Compression Active(3)	Out	55
$\overline{ERR}$	Error detected by MNP(3)	Out	54

89C026LT PINOUT (Continued)

Symbol	Function (89C026LT)	Direction(4)	Pin No.
NMI	Non-maskable Interrupt(V_{SS})(1)	In	3
X2	Crystal output	Out	66
CLKOUT	Clk output	Out	65
BUSWIDTH	Bus Width	In	64
INST	External memory instruction fetch	Out	63
ALE	Address latch enable	Out	62
$\overline{RD}$	External memory read	Out	61
READY	External memory ready	In	43
$\overline{BHE}$	External memory bus high enable	Out	41
$\overline{WR}$	External memory write	Out	40

NOTES:
1. Pins marked with (V_{SS}) must be connected to V_{SS}.
2. Pins marked with (V_{CC}) must be connected to V_{CC}.
3. AD0–AD3 are used as $\overline{AA}$, $\overline{JS}$, $\overline{CD}$, $\overline{MR}$, $\overline{REL}$, $\overline{CLASS\ 5}$, and $\overline{ERR}$ respectively.
4. Pins with direction "IN" must not be left floating.

89C026LT PIN DESCRIPTION

$\overline{XTCLK}$

Transmitter timing from DTE, when external clock option is selected.

TXD

The serial data from DTE to be transmitted on the line. A logic 'high' is mark. In synchronous mode, 89C026LT samples this data on the rising edges of $\overline{TCLK}$.

$\overline{TCLK}$

Clock output from 89C026LT as timing source for data exchange from DTE to modem. Serial data is read on the rising edges of the $\overline{TCLK}$. This output is High in asynchronous mode.

RXD

The serial data to DTE. A logic 'high' is mark. In synchronous mode, the rising edge of $\overline{RCLK}$ occurs in the middle of RXD.

$\overline{RCLK}$

Synchronous clock output. Rising edge of $\overline{RCLK}$ occurs in the middle of each RXD bit. This pin remains High in asynchronous mode.

$\overline{PD}$

Power-down control. A low on this input pin, in conjunction with the +En and +Tn commands, will cause the modem to go into a power-down mode.

V_{PP}

Timing pin for return from power-down. Connect a 1.0 μf capacitor between V_{PP} and V_{SS} if the power-down option is used. This capacitor causes an internal timing circuit to give the oscillator time to stabilize before turning on internal clocks. This pin may be left floating or connected through a 1.0 μF capacitor to V_{SS} if power-down mode is not required.

$\overline{TM}$

A low indicates maintenance condition in the modem.

$\overline{DCD}$

In async operation, $\overline{DCD}$ remains low regardless of data carrier (default), or it can be programmed to indicate received carrier signal is within the required timing and amplitude limits. In sync operation low indicates the received carrier signal is within the required timing and amplitude limits.

$\overline{DSR}$

A low indicates modem is off-hook, is in data transmission mode, and the answer tone is being exchanged. $\overline{CTS}$ low indicates modem is prepared to accept data.

$\overline{RTS}$

In async mode $\overline{RTS}$ is ignored. Under command control, in sync mode $\overline{RTS}$ can be ignored, or the modem can respond with a Low on $\overline{CTS}$.

$\overline{DTR}$

&D0 command will cause the modem to ignore $\overline{DTR}$. For &D1 the modem assumes the asynchronous command state on a low-to-high transition of the $\overline{DTR}$ circuit. The &D2 command does the same as &D1 except the state of $\overline{DTR}$ will enable/disable auto answer. A low-to-high transition of $\overline{DTR}$ after the &D3 command will cause the modem to assume the initialization state.

TCL1, TCL0

These pins are used as the serial clock and data for interface to an NVRAM. Refer to Figure 3. TCL0 is used to output a clock and serial data is transferred in on TCL1.

$\overline{AR}$

This Auxiliary relay control is for switching a relay for voice or data calls. High is voice, low is data.

$\overline{RI}$

A low signal from DAA indicates line ringing. This input is ignored when the modem is configured for leased line. This signal should follow the ring cadence.

$\overline{OH}$

Low sets an off hook condition, high indicates an on hook. When dialing, this signal is used to pulse dial the line.

$\overline{SH}$

Used as a telephone voice to data switch or vice versa. Any logic level transition will toggle the modem state between voice and data.

$\overline{AA}$

Used as an indicator for Auto Answer status and Ring indicator. Active low.

$\overline{LCLLB}$

A low will set the modem in the local analog loopback test mode. Logic Low levels applied simultaneously to $\overline{REMLB}$ and $\overline{LCLLB}$ pins, sets the modem to the local digital loopback.

$\overline{REMLB}$

A low on this pin initiates a remote loopback condition.

$\overline{CD}$

A Low indicates the presence of carrier signal on the line.

$\overline{MR}$

A low indicates the presence of the DSR signal. Toggling indicates that a test mode is active.

$\overline{REL}$

A low indicates that an MNP reliable link has been established.

$\overline{CLASS5}$

A low indicates that MNP Class 5 (data compression) is in operation.

$\overline{ERR}$

Goes low for 1 second whenever MNP detects an error.

$\overline{SI}$

Selects one of the two data rates or ranges of rates in the DTE to correspond to the rate in modem. Low selects the higher rate (2400 CCITT/1200 BELL) or range of rates. High selects the Low rate or range of rates.

D/$\overline{S}$

A low on this pin will indicate the smart mode which will respond to all commands. A High will ignore all commands.

V_{REF}

Voltage reference for the analog to digital converter should be connected to the 89027 AVcc.

V_{SS}

This pin must be connected to Digital Ground.

S/$\overline{A}$

The function of this pin is re-defined as external NVRAM CE.

CONFIG

Reserved for future use. This signal should be pulled high.

$\overline{EA}$

When high, memory access from address 2000H to 4000H are directed to on-chip ROM. When low, all Memory access is directed to off-chip memory. This pin must be tied high.

$\overline{JS}$

Low is used to pulse A and A1 leads to control a 1A2 Key System jack.

BUSWIDTH

When high, external memory accesses are 16 bits wide. When low, external memory accesses are 8 bits wide. This pin must be tied low.

READY

When high, no wait states are inserted in external memory accesses. When low, one wait state is inserted in each external memory access.

89C026LT ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature ..... −40°C to +125°C
Voltage from Any Pin to
V_{SS} or AGND ..... −0.5V to +7.0V
Average Output Current from Any Pin ..... 10 mA
Power Dissipation ..... 1.5 Watts

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature Under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	4.75	5.25	V
V_{REF}	Analog Supply Voltage	4.75	5.25	V
f_{OSC}	CLKIN Frequency	12.95870	12.96130	MHz

NOTE:
The AGND and V_{SS} on both the 89C026LT and the 89027 must be nominally at the same potential.

DC CHARACTERISTICS

Symbol	Parameter	Min	Typ(7)	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5		+0.8	V	
V_{IH}	Input High Voltage(1)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage on CLKIN	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{IH2}	Input High Voltage on RESET	2.6		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage			0.3 0.45 1.5	V V V	I_{OL} = 200 μA I_{OL} = 3.2 mA I_{OL} = 7 mA
V_{OH}	Output High Voltage(4)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −200 μA I_{OH} = −3.2 mA I_{OH} = −7 mA
V_{OH1}	Output High Voltage(3)	V_{CC} − 0.3 V_{CC} − 0.7 V_{CC} − 1.5			V V V	I_{OH} = −10 μA I_{OH} = −30 μA I_{OH} = −60 μA
I_{LI}	Input Leakage Current(5)			±10	μA	$0 < V_{IN} < V_{CC} - 0.3V$
I_{LI1}	Input Leakage Current(6)			±3	μA	$0 < V_{IN} < V_{REF}$
I_{IL}	Logical 0 Input Current(3)			−50	μA	V_{IN} = 0.45V
I_{IL1}	Logical 0 Input Current in RESET(2) (ALE, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, INST, SCLK)			−7	mA	V_{IN} = 0.45V

DC CHARACTERISTICS (Continued)

Symbol	Parameter	Min	Typ(7)	Max	Units	Test Conditions
I_{REF}	A/D Converter Reference Current		2	5	mA	CLKIN = 12.96 MHz $V_{CC} = V_{PP} = V_{REF} = 5.25$
I_{CC1}	Active Mode Current (Typical)		45	60	mA	CLKIN = 12.96 MHz
R_{RST}	RESET Pullup Resistor	6K		50K	Ω	
C_S	Pin Capacitance (Any Pin to V_{SS})			10	pF	f_{TEST} = 1.0 MHz
I_{PD}	Power-Down Mode Current		5	50	μA	$V_{CC} = V_{PP} = V_{REF} = 5.25$

NOTES:
(Notes apply to all specifications)
1. All pins except RESET and CLKIN.
2. Holding these pins below V_{IH} in RESET may cause the part to enter test modes.
3. TCL0, TCL1, S/$\overline{A}$, RTS, $\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, $\overline{SI}$, $\overline{OH}$.
4. $\overline{BHE}$, INST, CLKOUT, RESET, $\overline{TCLK}$, RXD, $\overline{RCLK}$, TSYNC, $\overline{TM}$, SCLK, SDATA. The V_{OH} specification is not valid for RESET.
5. EA, READY, BUSWIDTH, NMI, STR, DTR, XTCLK, TXD, B/C, CLKIN2, and RI.
6. S/D, $\overline{SH}$, $\overline{REMLB}$, $\overline{LCLLB}$, I, Q, CONFIG, ED.
7. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC} = 5V$.

AC CHARACTERISTICS (Over specified operating conditions)

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, f_{OSC} 12.96 MHz

This system must meet these specifications to work with 89C026LT:

Symbol	Parameter	Min	Max	Units	Notes
T_{AVYV}	Address Valid to READY Setup		$2T_{OSC} - 75$	ns	
T_{LLYV}	ALE Low to READY Setup		$T_{OSC} - 60$	ns	
T_{YLYH}	Non READY Time	No Upper Limit		ns	
T_{CLYX}	READY Hold after CLKOUT Low	0	$T_{OSC} - 30$	ns	(Note 1)
T_{LLYX}	READY Hold after ALE Low	$T_{OSC} - 15$	$2T_{OSC} - 40$	ns	(Note 1)
T_{AVGV}	Address Valid to Buswidth Setup		$2T_{OSC} - 75$	ns	
T_{LLGV}	ALE Low to Buswidth Setup		$T_{OSC} - 60$	ns	
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns	
T_{AVDV}	Address Valid to Input Data Valid		$3T_{OSC} - 55$	ns	(Note 2)
T_{RLDV}	$\overline{RD}$ Active to Input Data Valid		$T_{OSC} - 23$	ns	(Note 3)
T_{CLDV}	CLKOUT Low to Input Data Valid		$T_{OSC} - 50$	ns	
T_{RHDZ}	End of $\overline{RD}$ to Input Data Float		$T_{OSC} - 20$	ns	
T_{RXDX}	Data Hold after $\overline{RD}$ Inactive	0		ns	

NOTE:
1. If max is exceeded, additional wait states will occur.
2. $T_{AVDV} = 3T_{OSC} - 67 + 2T_{OSC}$ (for 1 wait state)
3. $T_{RLDV} = T_{OSC} - 23 + 2T_{OSC}$ (for 1 wait state)

AC CHARACTERISTICS (Continued)

Test Conditions: Capacitive load on all pins = 100 pF, Rise and fall times = 10 ns, f_{OSC} 12.96 MHz

The 89C026LT will meet these specifications:

Symbol	Parameter	Min	Max	Units	Notes
F_{CLKIN}	Oscillator Frequency	12.95870	12.96130	MHz	
T_{OSC}	Oscillator Period	$1/F_{CLKIN(MAX)}$	$1/F_{CLKIN(MIN)}$	ns	
T_{XHCH}	F_{CLKIN} High to CLKOUT High or Low	40	110	ns	(Note 1)
T_{CLCL}	CLKOUT Cycle Time	2 T_{OSC}		ns	
T_{CHCL}	CLKOUT High Period	T_{OSC} − 10	T_{OSC} + 10	ns	
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	−10	10	ns	
T_{LLCH}	ALE Falling Edge to CLKOUT Rising	−15	15	ns	
T_{LHLH}	ALE Cycle Time	4 T_{OSC}		ns	
T_{LHLL}	ALE High Period	T_{OSC} − 10	T_{OSC} + 10	ns	
T_{AVLL}	Address Setup to ALE Falling Edge	T_{OSC} − 20		ns	
T_{LLAX}	Address Hold after ALE Falling Edge	T_{OSC} − 40		ns	
T_{LLRL}	ALE Falling Edge to $\overline{RD}$ Falling Edge	T_{OSC} − 35		ns	
T_{RLCL}	$\overline{RD}$ Low to CLKOUT Falling Edge	4	25	ns	
T_{RLRH}	$\overline{RD}$ Low Period	T_{OSC} − 5	T_{OSC} + 25	ns	
T_{RHLH}	$\overline{RD}$ Rising Edge to ALE Rising Edge	T_{OSC}	T_{OSC} + 25	ns	(Note 2)
T_{RLAZ}	$\overline{RD}$ Low to Address Float		10	ns	
T_{LLWL}	ALE Falling Edge to $\overline{WR}$ Falling Edge	T_{OSC} − 10		ns	
T_{CLWL}	CLKOUT Low to $\overline{WR}$ Falling Edge	0	25	ns	
T_{QVWH}	Data Stable to $\overline{WR}$ Rising Edge	T_{OSC} − 23		ns	
T_{CHWH}	CLKOUT High to $\overline{WR}$ Rising Edge	−5	15	ns	
T_{WLWH}	$\overline{WR}$ Low Period	T_{OSC} − 15	T_{OSC} + 5	ns	
T_{WHQX}	Data Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 15		ns	
T_{WHLH}	$\overline{WR}$ Rising Edge to ALE Rising Edge	T_{OSC} − 15	T_{OSC} + 10	ns	(Note 2)
T_{WHBX}	$\overline{BHE}$, INST, Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 15		ns	
T_{RHBX}	$\overline{BHE}$, INST, Hold after $\overline{RD}$ Rising Edge	T_{OSC} − 10		ns	
T_{WHAX}	AD8–15 Hold after $\overline{WR}$ Rising Edge	T_{OSC} − 30		ns	
T_{RHAX}	AD8–15 Hold after $\overline{RD}$ Rising Edge	T_{OSC} − 25		ns	

NOTES:
1. Typical specifications, not guaranteed.
2. Assuming back-to-back bus cycles.

WAVEFORMS

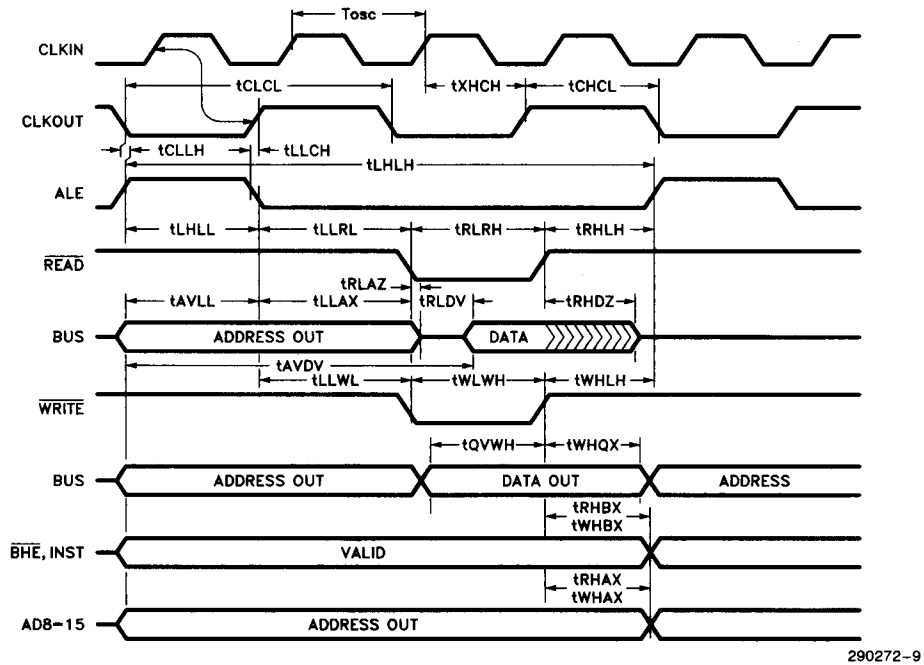

Figure 8. Bus Signal Timings

89027 OVERVIEW

The 89027 is a 28 pin CHMOS analog front end device, which performs most of the complex filtering functions required in modem transmitters and receivers. A general block diagram of this chip is provided in Figure 9. Most of the analog signal processing functions in this chip are implemented with CHMOS switched capacitor technology. The 89027 functions are controlled by 89C026LT, through a high speed serial data link.

During FSK transmit operation, the 89027 receives digitally synthesized mark and space sinusoid amplitude information from the 89C026LT. The 89027 converts the signal to its analog equivalent, filters it, and transmits it to the telephone line. For QAM transmission, the signal constellation points are transferred to the 89027. This information is modulated into an analog signal, passed through spectral shaping filters, combined with the necessary guard tone, smoothed by a low pass filter, and transmitted to the line. Prior to transmitting either FSK or QAM signals to the telephone line, the 89027 adjusts the signal gain through an on-board programmable gain amplifier.

During the receive operation, the received FSK and QAM signals are passed through anti-alias filters, bandsplit filters, automatic gain control and carrier detect circuits, a Hilbert transform filter, and the output sent to the 89C026LT processor as analog signals.

Other functions provided by the 89027 are: an on-board two wire to four wire circuit with disable capability, an audio monitor output with software configurable gain, and a programmable gain transmit signal.

The 89027 is available in 28 pin plastic DIP and PLCC packages.

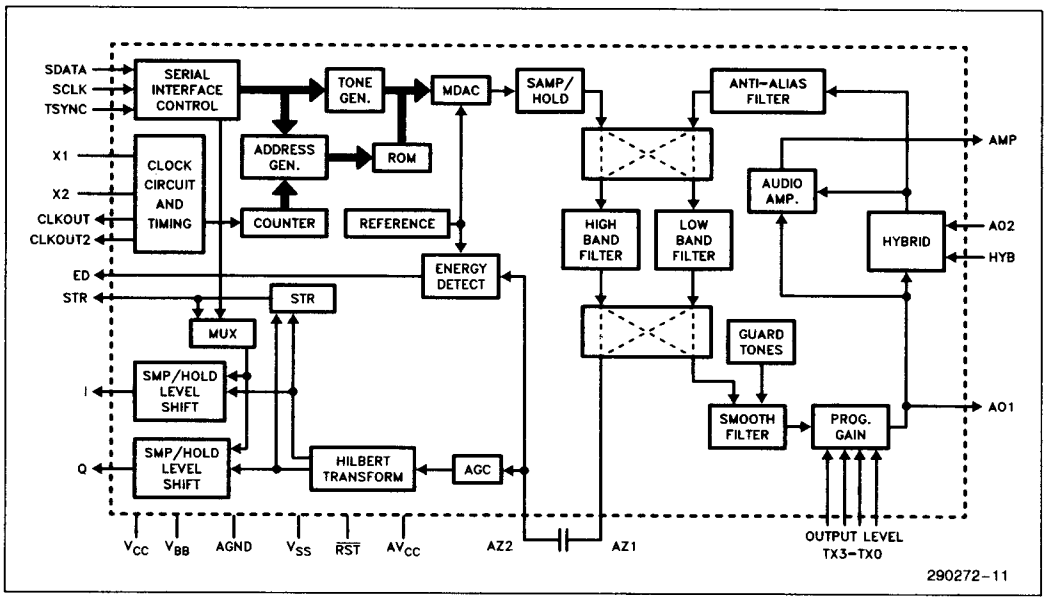

Figure 9. 89027 Block Diagram

89027 PINOUT

Symbol	Function (89027)	Direction	Pin No.
V_{CC}	Positive Power Supply (Digital)	+5V	28
V_{BB}	Negative Power Supply	−5V	15
V_{SS}	Digital Ground	DGND	24
AGND	Analog Ground	AGND	21
AV_{CC}	Positive Power Supply (Analog)	+5	7
X1	Xtal Oscillator	In	23
X2	Xtal Oscillator	Out	25
CLKOUT	12.96 MHz Clock Output to 89C026LT	Out	26
CLKOUT2	270 KHz Clock Output to 89C026LT	Out	19
$\overline{RST}$	Chip reset (active low)(3)	In	20
HYB	Enable on-chip hybrid(1)	In	10
AZ1	Auto-zero capacitor	Out	16
AZ2	Auto-zero capacitor	In	17
SDATA	Serial data from 89C026LT	In	2
SCLK	Serial clock from 89C026LT	In	1
TSYNC	Transmitter sync from 89C026LT	In	3
STR	Symbol timing to 89C026LT	Out	27
ED	Receiver energy detect to 89C026LT	Out	18
I	In phase received signal to 89C026LT	Out	13
Q	Quadrature-phase received signal to 89C026LT	Out	14
AO1	Transmitter output	Out	6
AO2	Receiver input	In	12
AMP	Output to monitor speaker	Out	11
TX0	Transmitter level control (LSB)(1)	In	9
TX1	Transmitter level control(1)	In	8
TX2	Transmitter level control(1)	In	5
TX3	Transmitter level control (MSB)(1)	In	4
NC	(Note 2)	In	22

NOTE:
1. When held high, these pins must be connected through 10K resistors to V_{CC}.
2. Reserved Pin. Must be left No Connect.
3. Connect to reset circuitry through a 10K resistor.

89027 Pinout Description

TX0-3

These four pins control the transmitted signal level. Refer to Transmit Level Table.

HYB

This pin enables the on-chip hybrid. A line impedance matching network must be connected between AO1 and AO2 when HYB is enabled. If HYB is disabled and an external 4W/2W hybrid is used, the hybrid receive path must be amplified by 6 dB.

AO1

Transmitter output.

AO2

Receiver input.

AMP

This output can be used to monitor the call progress tones and operation of the line.

ABSOLUTE MAXIMUM RATINGS(2)

Temperature Under Bias ..... 0 to +70° C
Storage Temperature ..... −40 to +125° C
All Input and Output Voltages with Respect to V_{BB} ..... −0.3V to +13.0V
All Input and Output Voltages with Respect to V_{CC} & AV_{CC} ..... −13.0V to 0.3V
Power Dissipation 1.35W
Voltage with Respect to V_{SS}(1) ..... −0.3V to 6.5V

NOTES:
1. Applies to pins SCLK, SDATA, TSYNC, $\overline{RST}$, HYB, TX0–TX3 only.
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature Under Bias	0	+70	°C
V_{CC}	Digital Supply Voltage	4.75	5.25	V
V_{BB}	Analog Supply Voltage	−4.75	−5.25	V

POWER DISSIPATION Ambient Temp = 0° to 70° C, V_{CC} = AV_{CC} = 5 ± 5%, V_{SS} = AGND = 0V.

Symbol	Parameter	Min	Typ	Max	Units
$AIcc_1$	AV_{CC} Operating Current		15	21	mA
Icc_1	V_{CC} Operating Current		5	6	mA
Ibb_1	V_{BB} Operating Current		−15	−21	mA
$AIcc_s$	AV_{CC} Standby Current		0.2	1	mA
Icc_s	V_{CC} Standby Current		5	6	mA
Ibb_s	V_{BB} Standby Current		−0.6	−2	mA
$AIcc_p$	AV_{CC} Power-Down Current		100		μA
Icc_p	V_{CC} Power-Down Current		450		μA
Ibb_p	V_{BB} Power-Down Current		450		μA
Pdo	Operating Power Dissipation		175	250	mW
Pds	Standby Power Dissipation		30	50	mW
Pd_p	Power Down Power Dissipation		5		mW

D.C. CHARACTERISTICS (T_A=0°C to 70°C, AV_{CC} = V_{CC} = 5V ±5%, V_{BB} = 5V ±5%, AGND = V_{SS} = 0V), supply voltage must be at the same potential as the 89C026LT power supply. Typical Values are for T_A = 25°C and nominal power supply values. V_{CC}, and AV_{CC}. V_{CC}, AV_{CC} and 89C026LT V_{REF} must be nominally at the same potential.

Inputs: TX0, TX1, TX2, TX3, HYB, $\overline{RST}$
Outputs: CLKOUT

Symbol	Parameter	Min	Max	Units	Test Conditions
Iil	Input Leakage Current	−10	+10	μA	$V_{SS} \leq Vin \leq V_{CC}$
Vil	Input Low Voltage	V_{SS}	0.8	V	
Vih	Input High Voltage	2.4	V_{CC}	V	
Vol	Output Low Voltage		0.4	V	Iol ≥ −1.6mA,1 TTL load
Voh	Output High Voltage	2.4		V	Ioh ≤ 50μa, 1 TTL load
Vcol	CLKOUT Low Voltage		0.4	V	Load Capacitance = 60 pF
Vcoh	CLKOUT High Voltage	0.7 V_{CC}		V	Load Capacitance = 60 pF

1

A.C. CHARACTERISTICS (T_A = 25°C, V_{CC} = AV_{CC} = 5V, V_{SS} = AGND = 0V, V_{BB} = −5V)

ANALOG INPUTS: AO2

Parameter	Min	Typ	Max	Units	Test Condition
AO2 Receive Signal Level			−9	dBm	Hybrid Enabled
AO2 Input Resistance		10		MOhms	−2.5V<Vin<+2.5V
AO2 Allowed DC offset	−30		+30	mV	Relative to AGND

AUTO ZERO CAPACITANCE

Capacitance = 0.015 μF
Tolerance = ±20%
Voltage Rating = 10V
Type = Non-Electrolytic, low leakage.

CRYSTAL REQUIREMENTS(1)

Parameter	Min	Typ	Max	Units	Comments
Frequency Accuracy (0°C–70°C)	−0.0035%	12.96	+0.0035%	MHz	Refer to Figure 10
Rx		10	16	Ohms	
Cx		0.024		pF	
Co	5.1	5.6	6.1	pF	
C_L(2)	−5%	47	+5%	pF	2 Load Capacitors

NOTES:
1. Crystal Type: Parallel Resonant
2. Crystal manufacturers usually specify the accuracy of a parallel resonant circuit at a given "load capacitance". This "load capacitance" is specified to the crystal manufacturer as 33 pf. 33 pf includes the parallel combination of the capacitances seen at the pins of the crystal. These capacitances include C_L, IC pin capacitances, and a 3 ± 2 pf trace capacitance.

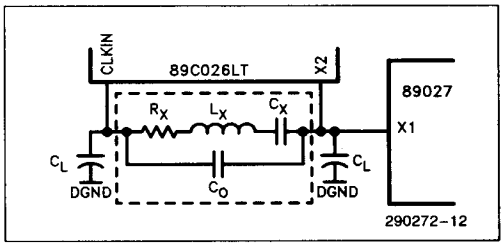

Figure 10. Crystal Equivalent Circuit

ANALOG OUTPUTS: A01, AMP

Parameter	Min	Typ	Max	Units	Comments
Load Resistance AO1 AMP	 600 10			 Ohms kOhms	
Load Capacitance AMP			 100	 pF	
Audio Amp Gain AO1 to Amp		−9 −18 −26 −70		dB dB dB dB	Max Mid (Software Selectable) Min Off
Audio Amp Gain(1) AO2 to Amp		+12 +3 −4 −60		dB dB dB dB	Max Mid (Software Selectable) Min Off

NOTE:
1. Assumes on-chip hybrid is enabled. When on-chip hybrid is disabled, gain with respect to AO2 is reduced by 6 dB.

Transmit Output Level(1)		
TX 3,2,1,0	Typ	Units
0 0 0 0	+5	dBm
0 0 0 1	+4	dBm
•	•	•
•	•	•
•	•	•
1 1 1 0	−9	dBm
1 1 1 1	−10	dBm

NOTE:
1. For PSK and QAM transmit signal. For FSK transmit signal levels, they are typically 1 dB lower. All signals are measured at A01. The tolerance for the transmit levels is ±1 dBm.

Reference Manuals

The Modem Reference Manual (Order Number 296235-002) contains pin descriptions, AT and MNP command descriptions, schematics, and important design guidelines for the 89C024LT, 89C024XE, and 89024 modem chip sets. The Modem Software Reference Manual (Order Number 296503-001) provides information about the modem software routines. Contact your local Intel sales office for the latest information.

89C024XE CHIP SET USERS:

Note the following when using the 89C024LT Laptop chip set in place of the 89C024XE:

1. $\overline{PD}$ (B/$\overline{C}$ on 89C024XE) can be left tied to digital V_{CC} or can be connected to the power-down control. If the power down mode is used, a 1.0 μf capacitor must be connected from V_{PP} on the 89C026LT to digital ground.
2. Buswidth pin is tied directly to ground because 89C024LT uses 8-bit EPROM.
3. No 74HC373 latch is required for AD8–AD15 because 89C026LT latches them internally.
4. A single chip select inverter is required from AD15 to select between EPROM and RAM memory.
5. Optional inverter from AD14 can be used to power-down RAM.
6. If minimum power-down currents are not required, the 89C024XE crystal configuration and specifications may be used.

REVISION SUMMARY

The following list represents the differences between version -005 and version -004 of the 80C024LT Error Correcting Laptop Modem Chip Set Data Sheet. These changes reflect the device characteristics changes due to the P645 to P629.1 process conversion.

Packaging

In Figure 3., Device Packages, pin 14, Clock Detect Enable (CDE), has been changed to V_{SS}.

Applications Overview

In Figure 4., Typical Laptop Modem, CDE has been changed to V_{SS}.

89C026LT Overview

In Figure 7., 89C026LT Block Diagram, CDE has been changed to V_{SS}.

89C026LT Pinout

CDE has been changed to V_{SS}.

89C026LT Pin Description

CDE has been changed to V_{SS}, and the paragraph is changed to say that this pin is connected to digital ground.

DC Characteristics

V_{IH1} Min has changed from 2.2V to 2.6V.
I_{IL1} Max has changed from −850 μA to −7 mA.
CDE has been removed from Note 5.

AC Characteristics

T_{AVYV} Max has changed from 2 T_{OSC} − 85 ns to 2 T_{OSC} − 75 ns.
T_{LLYV} Max has changed from T_{OSC} − 72 ns to T_{OSC} − 60 ns.
T_{AVGV} Max has changed from 2 T_{OSC} − 85 ns to 2 T_{OSC} − 75 ns.
T_{LLGV} Max has changed from T_{OSC} − 70 ns to T_{OSC} − 60 ns.

AC Characteristics (Continued)

T_{AVDV} Max has changed from 5 T_{OSC} − 67 ns to 3 T_{OSC} − 55 ns.
T_{RLDV} Max has changed from 3 T_{OSC} − 23 ns to T_{OSC} − 23 ns.
T_{CLLH} Min has changed from −5 ns to −10 ns, and the Max has changed from 15 ns to 10 ns.
T_{LLRL} Min has changed from T_{OSC} − 40 ns to − 35 ns.
T_{RLCL} Min has changed from 5 ns to 4 ns, and the Max has changed from 30 ns to 25 ns.
T_{CHWH} Min has changed from −10 ns to −5 ns, and the Max has changed from 10 ns to 15 ns.
T_{WLWH} Min has changed from T_{OSC} − 30 ns to T_{OSC} − 15 ns.
T_{WHQX} Min has changed from T_{OSC} − 10 ns to T_{OSC} − 15 ns.
T_{WHLH} Min has changed from T_{OSC} − 10 ns to T_{OSC} −15 ns, and the Max has changed from T_{OSC} + 15 ns to T_{OSC} + 10 ns.
T_{WHBX} Min has changed from T_{OSC} − 10 ns to T_{OSC} − 15 ns.
T_{WHAX} Min has changed from T_{OSC} − 50 ns to T_{OSC} − 30 ns.